# Static Upset Characteristics of the 90nm Virtex-4QV FPGAs

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***Abstract*—Radiation Test Consortium (XRTC) single-event measurements for three of the latest generation of radiation-tolerant reconfigurable FPGAs from Xilinx (90nm, copper-interconnected, thin-epitaxial CMOS) are presented. Results include proton and heavy-ion upset susceptibilities for unclocked memory elements, high-temperature latchup immunity and a low SEFI rate (e.g., ~one/device-century in geosynchronous orbit).**

## I. Introduction

FIELD programmable gate arrays have proven over the years to be a practical and effective alternative to custom ASICs for space applications, winning on development cost and length of schedule while lagging on size and complexity. The march of Moore's law has brought us to the point where bigger and more complex designs can now be accomplished with current commercial FPGAs, as compared to available rad-hard ASICs. In this paper, we consider a specific sub-case of the general question: can commercial FPGAs (or devices leveraged off them) be demonstrated to have acceptable radiation characteristics?

## II. The Test Devices: XQR4VSX55, XQR4VFX60, and XQR4VLX200

The current "radiation tolerant" or "radiation hardened" FPGAs from Xilinx (which carry the "XQR" prefix) are typically a select subset of their counterparts in the corresponding commercial family with a few differences: they are (1) fabricated on thin epitaxial wafers from a distinct, mature mask set at a single foundry (UMC), (2) offered in high reliability packages, (3) subjected to high reliability process flows and screens and (4) come with guaranteed radiation specifications. Virtex-4 is the latest family to be offered as "XQR" components and they are offered as class "S" (equivalent, DSCC cert pending). At a 90nm process geometry, it is the most highly scaled CMOS technology offered to the aerospace community. The largest radiation-tolerant Virtex-4 FPGA is well over a billion transistors. Partly as an aid to help designers manage this level of complexity, Virtex-4 introduced larger hard-wired, programmable elements in three 'flavors' or platforms that tilt the balance of "hard IP" resources in different directions: LX has more of the traditional gate array fabric while SX facilitates DSP designs with hundreds of multiplier-accumulator blocks and FX supports heavy-duty processing tasks with embedded PowerPCs. Samples of all three platforms were irradiated for this work. Because this technology is only available in flip-chip packages, samples were thinned to ~80 μm of remaining substrate to allow beam penetration. Note that previous publications of Virtex-4 radiation results are for commercial (non-epi, "XC" prefix) devices [1-5], but [6] is a notable exception.

TABLE I
ARCHITECTURE RESOURCES OF THE VIRTEX-4 QV PRODUCT FAMILY

| | XQR4V... | | | |
|---|---|---|---|---|
| | ...SX55 | ...FX60 | ...FX140 | ...LX200 |
| CFG | 15.4 Mbits | 14.5 Mbits | 34.5 Mbits | 43.0 Mbits |
| BRAM | 5,898,240 | 4,276,224 | 10,174,464 | 6,193,152 |
| LOGIC | 24,576 | 25,280 | 63,168 | 89,088 |
| DSP | 512 | 128 | 192 | 96 |
| PPC | - | 2 | 2 | - |
| DCM | 12 | 12 | 20 | 12 |
| MGT | - | N/A | N/A | - |
| IOBs | 640 | 576 | 896 | 960 |

The abbreviations and acronyms in the first column of Table I are as follows: CFG stands for the SRAM configuration cells; BRAM is user block RAM, LOGIC resources are measured in "slices" with each one containing two lookup tables and two flip-flops; DSPs are 18x18 multiply-and-accumulate programmable blocks that enable digital signal processing applications; PPC stands for the embedded PowerPC405 blocks; DCMs are programmable digital clock manager blocks; and multi-gigabit transceivers or MGTs are high speed I/O pins while IOBs are the input/output blocks associated with normal speed I/Os. Note

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that MGTs are currently not officially supported due to operational difficulties at the extremes of the military temperature range (-55 to +125°C).

## III. Test Methodology

Testing was conducted with heavy ions by members of the Xilinx Radiation Test Consortium on SX55 samples in March 2007 at the Texas A & M University Cyclotron Institute (TAMU). Testing continued on SX55, FX60, and LX200 devices with heavy ions at TAMU in August 2007 and with protons at the University of California at Davis (UC-Davis) cyclotron in September 2007. The heavy-ion FX140 latchup test at TAMU was conducted in early August 2008, just in time for inclusion here.

Latchup testing was conducted with the highest available LETs with specification-maximum biases of $V_{CC}$=1.26V, $V_{IO}$ & $V_{AUX}$= 2.65V and at elevated temperatures obtained by running a "heater" design pre-beam. Static upset testing was done by loading a pattern into the subject memory cells (a design in the case of the configuration cells), irradiating it without clocking, and counting the number of bit flips after the beam is turned off. SEFI testing was done dynamically because it required monitoring a functioning design for various interruptions. In particular, the power-on-reset, POR, and the global signal or GSIG SEFIs result in an immediate problem with a design's operation. Alternatively, a SEFI is also declared when the ability to readback and/or scrub the configuration memory through the so-called SMAP port is interrupted. Note that hits on the frame address register or FAR are a specifically detectable subset of the SMAP SEFI.

## IV. Measured Cross Sections

### A. Latchup

The latchup data of Fig. 1 and Table II can be summarized succinctly – no latchup occurred for a total fluence of over $10^8$ ions/cm$^2$ of high LET ions on eight tested devices at high bias and high temperature. SEL testing on samples of the FX140 device will be conducted in the near future.

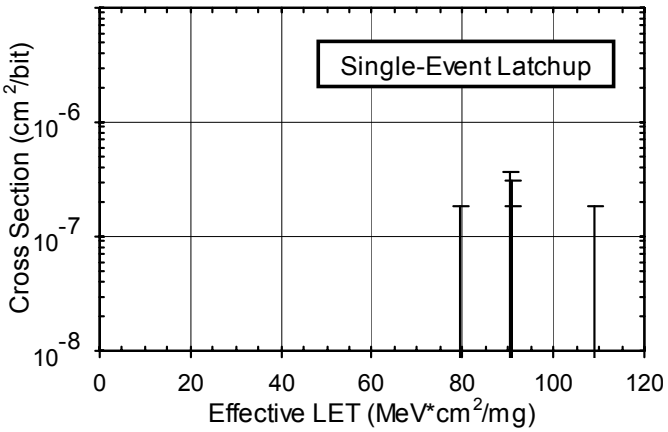



Fig. 1. A plot of the latchup data of Table II. Because no latchups were observed during these heavy ion tests, only the tops of the two-sigma statistical error bars are visible.

### B. Static Cell Upset

#### 1) Configuration Cells

As documented in Table I, the bulk of the storage cells for these FPGAs are the configuration SRAMs. Unlike conventional SRAMs where only one bit (or a few) are read at a time, the output of each configuration bit is always on, controlling a design level element, such as lookup table values and paths through the routing matrices. This output load combined with relaxed speed requirements relative to commercial 90nm SRAM devices (writing can be relatively leisurely since it is done rarely and read access times are meaningless) create the expectation that configuration cells should be somewhat harder to upset than its commercial SRAM array counterpart. The upset data confirms that expectation for heavy ions, but, surprisingly, the extra upset hardness seems to come not in LET threshold or the cross section at high LET, but in the knee between LET extremes.

Table II
Latchup Test Data from TAMU using 15 MeV/amu Ion Beams

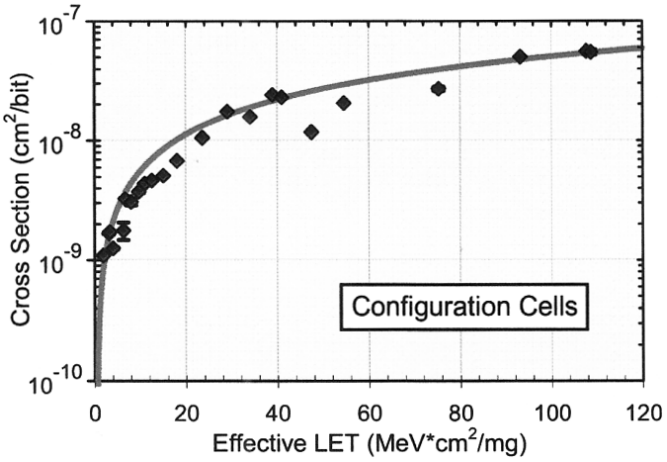
| Device | Ion | $LET_{eff}$ | Range, µm | Flux, #/ cm$^2$-s | Fluence, #/cm$^2$ | Start °C | End °C | SELs |
|---|---|---|---|---|---|---|---|---|
| **XQR4VSX55** | | | | | | | | |
| SN#A1443 | Au | 108.7 | 71.9 | $7.0 \times 10^4$ | $2.0 \times 10^7$ | 82 | 65 | None |
| SN#3 | Ho | 79.4 | 73 | $7.5 \times 10^4$ | $2.0 \times 10^7$ | 120 | 90 | None |
| **XQR4VFX60** | | | | | | | | |
| SN#601 | Au | 93.1 | 45 | $1.45 \times 10^4$ | $1.2 \times 10^7$ | 120 | 73 | None |
| SN#602 | Au | 90.8 | 75 | $8.42 \times 10^4$ | $2.0 \times 10^7$ | 120 | 88 | None |
| **XQR4VFX140** | | | | | | | | |
| SN#100 | Au | 93.5 | 55 | $1.13 \times 10^5$ | $2.0 \times 10^7$ | 127 | 105 | None |
| SN#80 | Au | 90.8 | 75 | $1.12 \times 10^5$ | $2.0 \times 10^7$ | 122 | 105 | None |
| SN#65 | Au | 88.7 | 90 | $2.24 \times 10^5$ | $4.0 \times 10^7$ | 124 | 105 | None |
| SN#65 | Au | 131.0 | 44 | $2.14 \times 10^5$ | $2.0 \times 10^7$ | 123 | 105 | None |
| **XQR4VLX200** | | | | | | | | |
| SN#554 | Au | 90.3 | 45 | $2.69 \times 10^4$ | $1.0 \times 10^7$ | 100 | 79 | None |

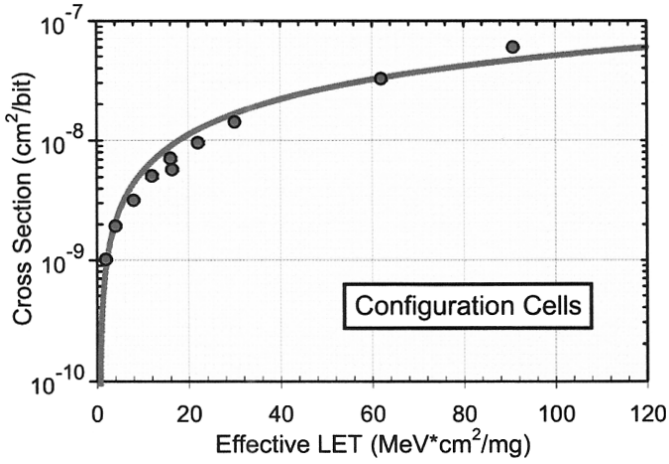
Units of $LET_{eff}$ are MeV per mg/cm$^2$

Configuration upset data for each of the three part types tested are shown in Fig. 2 for heavy ions and Fig. 3 for protons. Note that, although ~two sigma statistical error bars are plotted, they are difficult to see because they are generally smaller than the plotting symbols. The configuration SRAMs are implemented identically across the device types so one would expect that the upset susceptibilities would be identical except for statistical and part-to-part variations; indeed, a single Weibull curve for the heavy ion data and another for the proton data fit the all the data quite well.

#### 2) User Block RAM

Designers targeting Virtex-4QV devices have a moderately large quantity of memory available in the FPGA – over ten million bits in the XQR4VFX140. Thus, the upsetability of this user block RAM (or BRAM) is of definite interest. Further, these storage cells impact performance of a user design, and thus, they should be more like commercial SRAMs. Fig. 4 shows the results for the heavy ion irradiations while Fig. 5 shows the upset measurements for the proton runs. Note that no pattern dependence was seen.



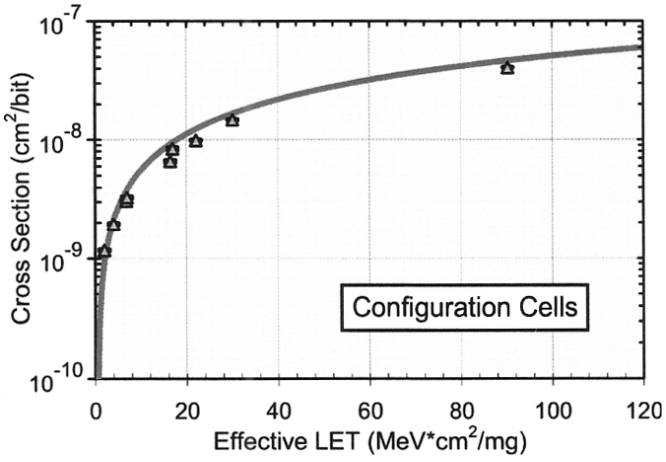
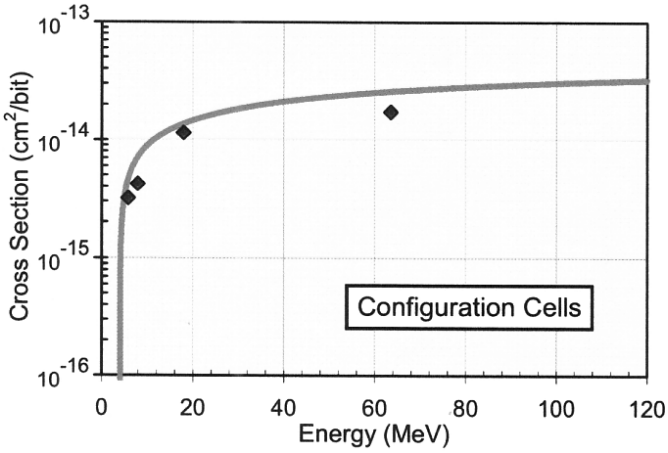
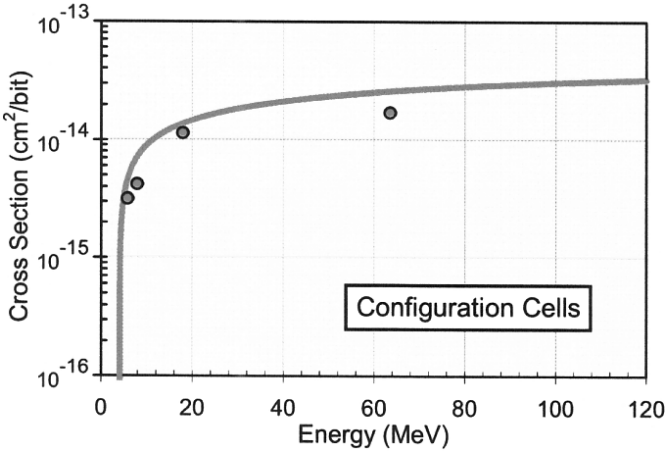




Fig. 2. Measured heavy-ion upset susceptibility of the configuration bits in Virtex-4QV's: (a) XQR4VSX55, (b) XQR4VFX60, and (c) XQR4VLX200. Two sigma statistical error bars are plotted, but are (mostly) not visible because they are smaller than the plotting symbol size. The Weibull curve shown has the following parameters: onset= 0.5 MeV per mg/cm$^2$, limit= 2.6x10$^{-7}$ cm$^2$/bit, width= 400, power= 0.985.



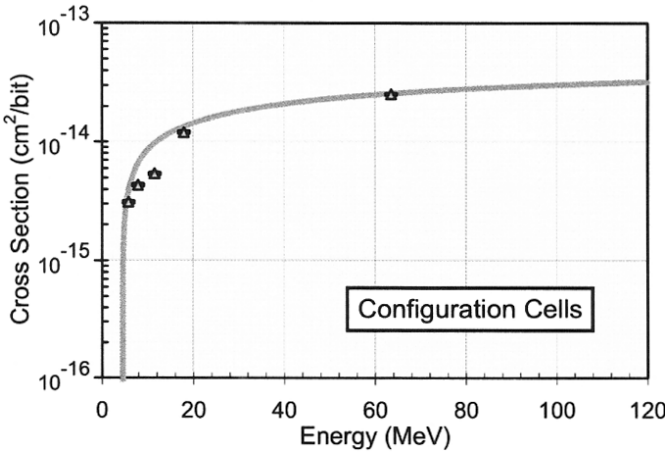




Fig. 3. Measured proton upset susceptibility of the configuration bits in Virtex-4QV's: (a) XQR4VSX55, (b) XQR4VFX60, and (c) XQR4VLX200. Two sigma statistical error bars are plotted, but are (mostly) not visible because they are smaller than the plotting symbol size. The Weibull curve shown has the following parameters: onset= 4 MeV, limit= 4.5x10$^{-14}$ cm$^2$/bit, width= 80, power= 0.586.

*3) User Flip-flops*

User flip-flops or design-level flip-flops are also susceptible to direct ionization upsets from heavy ion strikes and proton reaction products. Upsets in flip-flops tend to be of lesser importance than upsets in configuration and BRAM cells; part of the explanation is in the relative quantities - there are 1.3 to over 2 orders of magnitude fewer flops than BRAM storage cells and about 2.4 orders of magnitude fewer relative to configuration cells. For example, from Table I and the fact that there are two user flip-flops in every logic "slice," it is clear that the XQR4VLX200, the largest member of the Virtex-4QV family by this metric, has less than 200,000 (versus 43 million configuration bits, more than 240 times the number of user flip-flops).

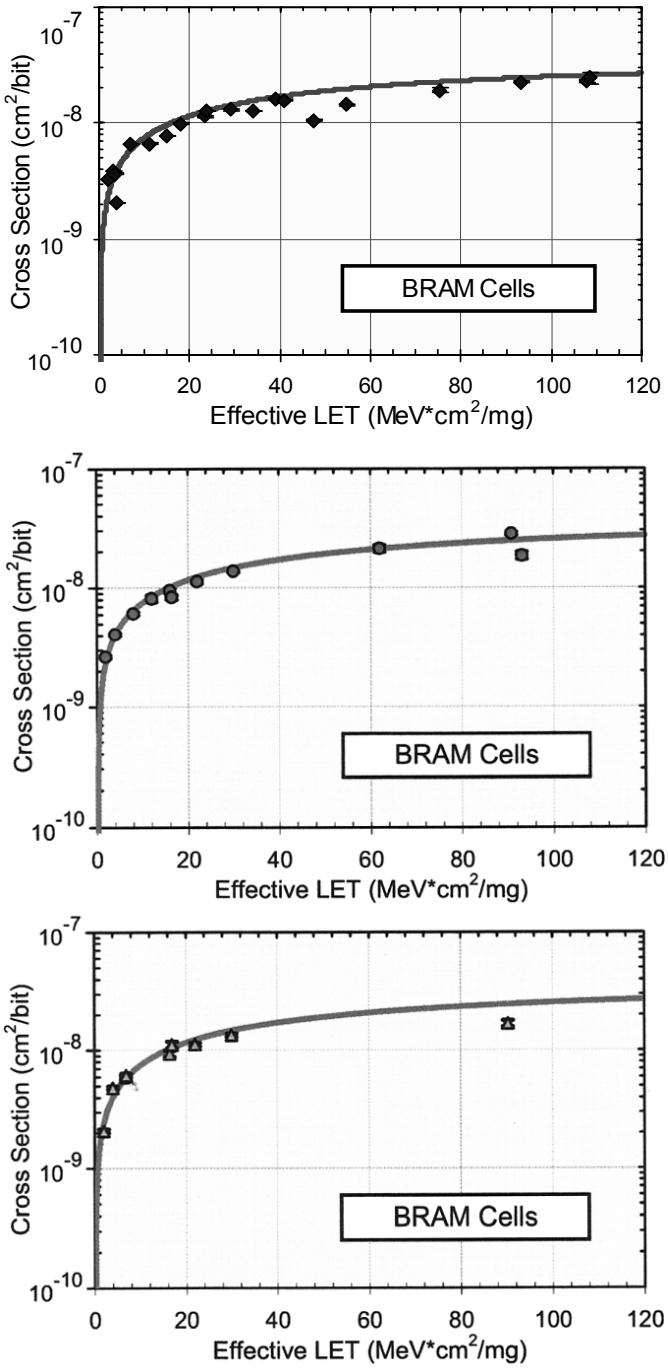



Fig. 4. Measurements of the heavy-ion upset susceptibility of BRAM bits in Virtex-4QV's: (a) XQR4VSX55, (b) XQR4VFX60, and (c) XQR4VLX200. No difference in cross section was observed between BRAMs storing zero vs. storing one. Two sigma statistical error bars are plotted, but are (mostly) not visible because they are smaller than the plotting symbol size. The Weibull curve shown has the following parameters: onset=0.2 MeV per mg/cm$^2$, limit=3.5x10$^{-8}$ cm$^2$/bit, width=70, power=0.724 .

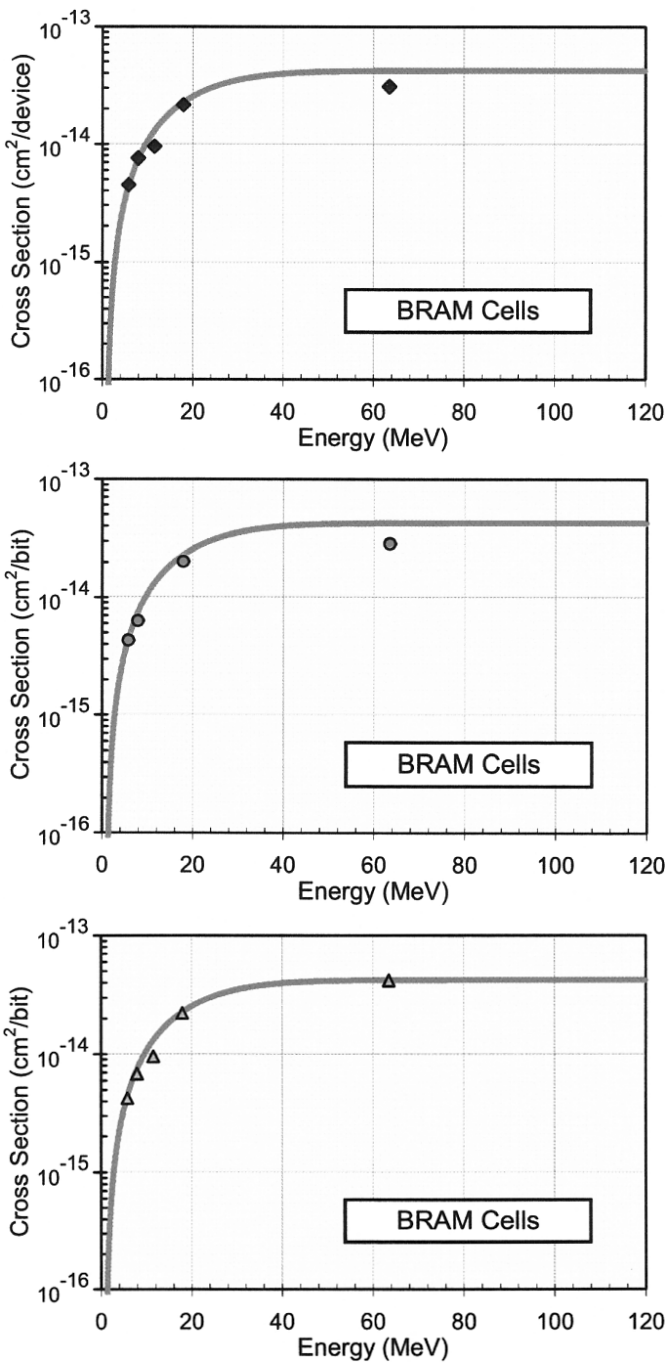
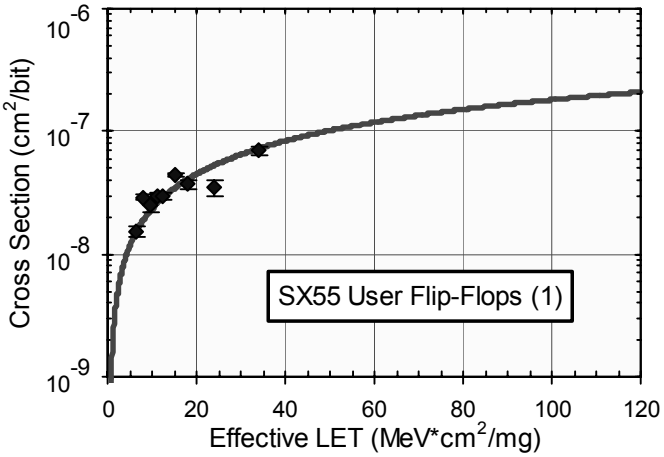



Fig. 5. Measurements of the proton upset susceptibility of BRAM bits in Virtex-4QV's: (a) XQR4VSX55, (b) XQR4VFX60, and (c) XQR4VLX200. No difference in cross section was observed between BRAMs storing zero vs. storing one. Two sigma statistical error bars are plotted, but are (mostly) not visible because they are smaller than the plotting symbol size. The Weibull curve shown has the following parameters: onset=1 MeV, limit=4.5x10$^{-14}$ cm$^2$/bit, width=20, power=1.546 .

The rest of the explanation is that indirect mechanism, that is configuration upsets and single-event transients are more likely to upset flip-flops, often in groups, than is direct ionization. In practice, this means that (1) flip-flop upset rates don't contribute significantly to the system error rate and that (2) flip-flop upset susceptibility is fairly difficult to measure. Earlier attempts to measure flip-flop static upset cross sections have resulted in consecutive identical irradiations that yielded upset counts that differed by up to two orders of magnitude. This indicates that "clobbers" or upsets of large groups of flip-flops from single ion strikes is contaminating the data.

A new approach to data collection was able to avoid the problem of large group errors. This approach involved running with low fluxes and effectively time tagging upsets as they happened. This allows the clobber counts to be



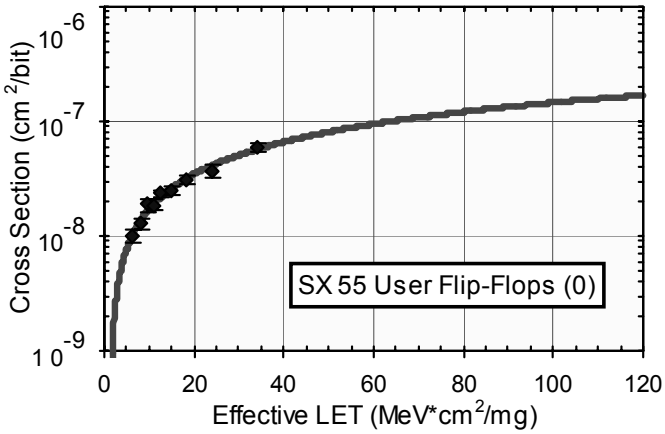
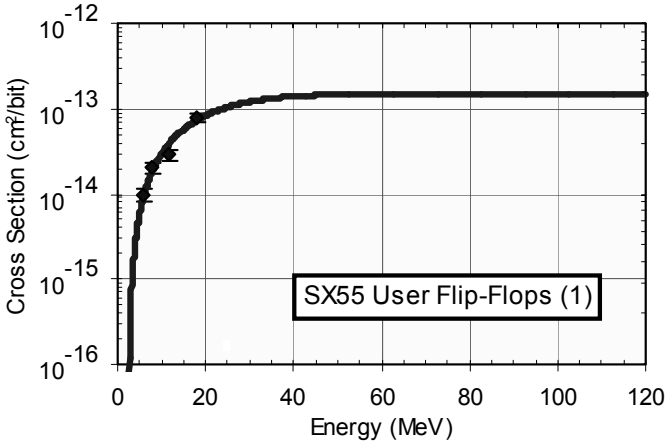




Fig. 6. Measured heavy-ion upset susceptibility of the user flip-flops in the XQR4VSX55. Note that the flip-flops are identical in the other members of the Virtex-4QV family: XQR4VFX60, XQR4VFX140, and XQR4VLX200. Two sigma statistical error bars are plotted, but are sometimes not visible because they are smaller than the plotting symbol size. The Weibull curves shown have the following parameters: for flip-flops storing one, onset= 0.5 MeV per mg/cm$^2$, limit= 7.5 x10$^{-7}$ cm$^2$/bit, width= 400, power= 0.923; for zero, onset= 1.5 MeV per mg/cm$^2$, limit= 6.1x10$^{-7}$ cm$^2$/bit, width= 400, power= 0.923. Note that, because the data covers only a limited range of LETs, the fits are more suggestive than definitive.



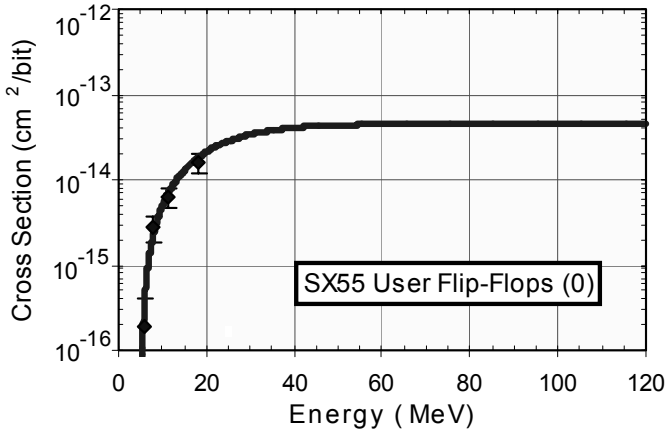




Fig. 7. Measured proton upset susceptibility of the user flip-flops in the XQR4VSX55. Note that the flip-flops are identical in the other members of the Virtex-4QV family: XQR4VFX60, XQR4VFX140, and XQR4VLX200. Two sigma statistical error bars are plotted. The Weibull curves shown have the following parameters: for flip-flops storing one, onset= 2.5 MeV, limit= 1.5 x10$^{-137}$ cm$^2$/bit, width= 20, power= 1.546; for zero, onset= 5 MeV per mg/cm$^2$, limit= 4.5x10$^{-14}$ cm$^2$/bit, width= 20, power= 1.546. Note that, because the data covers only a limited range of energies, the fits are more suggestive than definitive.

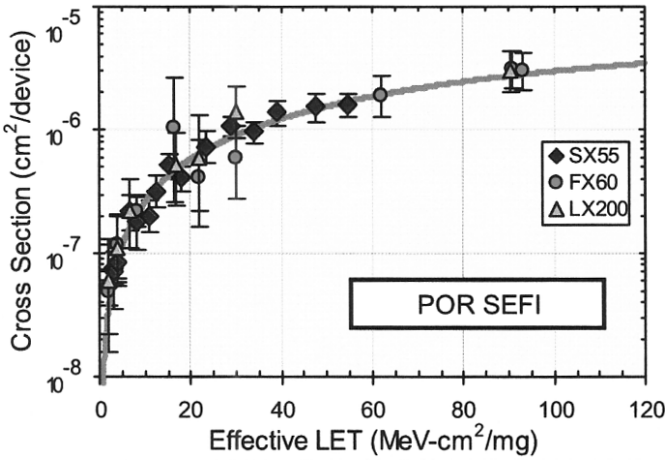
filtered out. While the remaining events that accumulated one or two at a time surely includes those caused by direct ionization, it is not clear how many indirect upsets it includes. Nevertheless, the heavy-ion data shown in Fig. 6 and the proton data of Fig. 7 represent the first time a reasonable and smooth dataset for user flip-flop upsets has been obtained. However, due to the lesser importance of direct flip-flop upsets, data collection was intentionally limited – the LET range covered was limited and only one device type (SX55) was tested. Note that the data shows flip-flops have a pattern-based asymmetry – they are easier to upset when storing the value 'one' than when storing 'zero.'

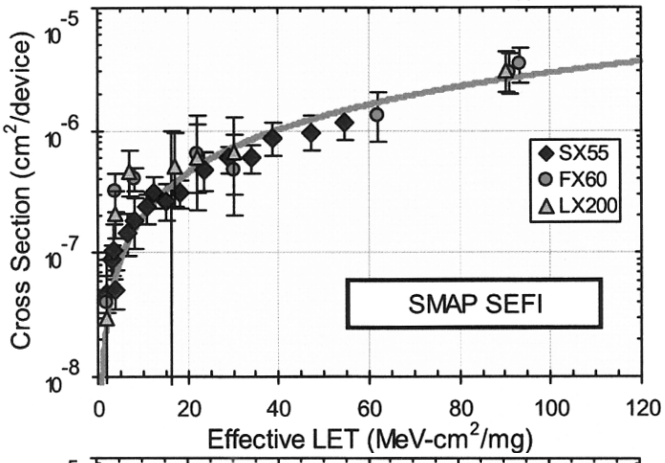
### *C. SEFIs*

Control registers and other SEFI susceptible areas are expected to be the same across all three sub-families of Virtex-4 devices. Both the heavy ion measurements shown in Fig. 8 and the proton data in Fig. 9 are consistent with that expectation. SEFI cross sections are so low that it is difficult to collect a statistically significant number of events in ground-based accelerator testing; thus, the ~two sigma statistical error bars shown are quite prominent. In collecting the proton data, two dozen samples were irradiated due to the total doses involved.

In addition to the three major SEFIs plotted in Fig. 8 and 9, three additional but smaller SEFIs were observed. The "global signal" or GSIG SEFI data collected were fit with Weibull curves with the following parameters: for heavy ions, onset=0.2 MeV per mg/cm$^2$, limit=2.01 x10$^{-7}$ cm$^2$/device, width=400, power=0.935; and for protons, onset=7.9 MeV, limit=2.2 x10$^{-12}$ cm$^2$/device, width=55, power=0.545.

The last two SEFI types, dubbed the readback or RB SEFI and the SCRUB SEFI, were so rare that the statistics are poor and cross section curves cannot be drawn without more extensive testing. Because they do not add significantly to the total SEFI rate, that additional effort was not undertaken; the current data set is more of an existence proof. The RB SEFI



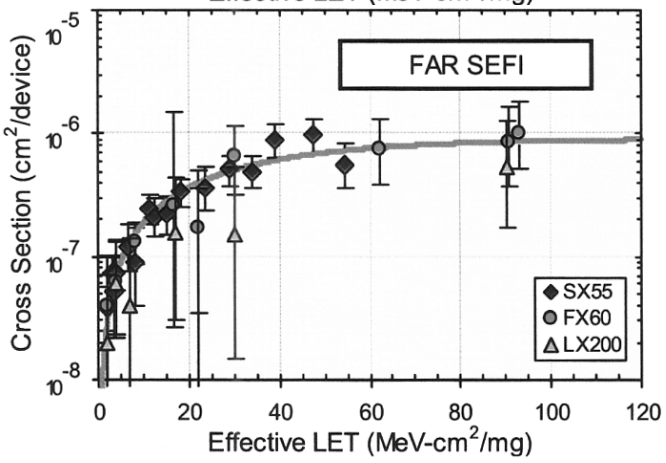
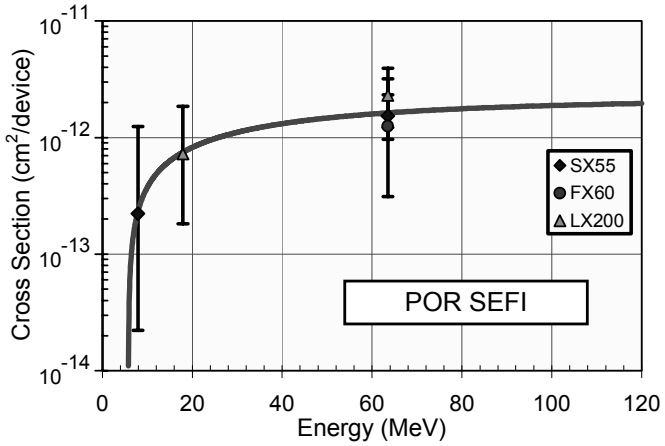
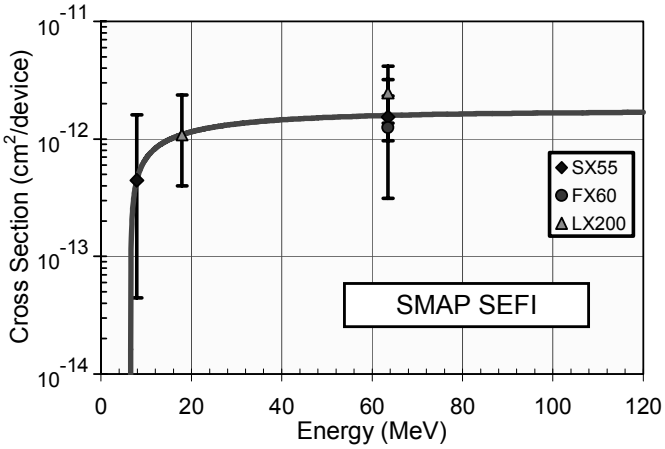




Fig. 8. Measured heavy-ion SEFI susceptibility in Virtex-4QV devices: XQR4VSX55, XQR4VFX60, and XQR4VLX200. Two sigma statistical error bars are plotted. The Weibull curves shown have the following parameters: for POR SEFIs, onset=0.2 MeV per mg/cm$^2$, limit=6.27 x10$^{-6}$ cm$^2$/device, width=150, power=1.169; for SMAP SEFIs, onset=0.2 MeV per mg/cm$^2$, limit=5.52 x10$^{-5}$ cm$^2$/device, width=1200, power=1.169; for FAR SEFIs, onset=0.2 MeV per mg/cm$^2$, limit=8.91 x10$^{-7}$ cm$^2$/device, width=35, power=1.127.



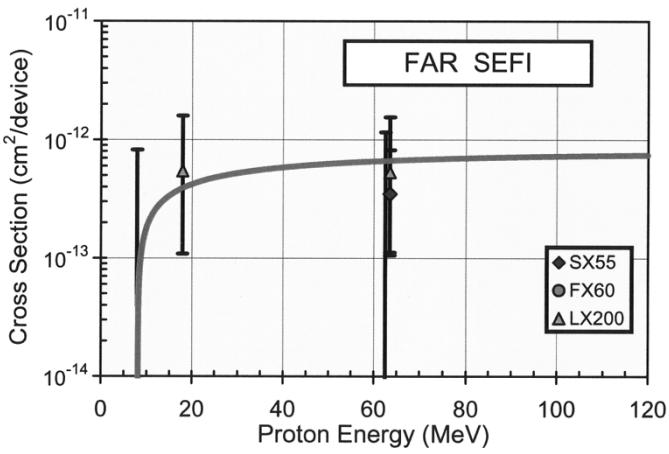




Fig. 9. Measured proton SEFI susceptibility in Virtex-4QV devices: XQR4VSX55, XQR4VFX60, and XQR4VLX200. Two sigma statistical error bars are plotted. The Weibull curves shown have the following parameters: for POR SEFIs, onset=5.8 MeV, limit=2.2 x10$^{-12}$ cm$^2$/device, width=40, power=0.760; for SMAP SEFIs, onset=6.5, limit=1.7 x10$^{-12}$ cm$^2$/device, width=10, power=0.568; for FAR SEFIs, onset=8.1 MeV, limit=3.3 x10$^{-13}$ cm$^2$/device, width=5, power=4.78.

is only a nuisance, in that the bits upset do not affect the design operation, but do complicate configuration management. The RB SEFI is now understood to result from the addition in Virtex-4 of configuration bits with two unusual characteristics: (1) they are "extras" in that they do not control any design elements and (2) they are not writeable.

In contrast, the SCRUB SEFI is thought to be the result of an upset during scrubbing that causes bad data to be written; this disrupts the design's operation, causes internal contention currents, and is the only SEFI observed whose cross section is dependent on the design under test.

A great deal of additional testing aimed at characterizing and understanding the SCRUB SEFI was undertaken by the

XRTC. In summary, there seems to be a correlation of the likelihood of SCRUB SEFI occurrence with number of ones in the configuration bitstream which is normally more than 90% zero, but the exact fraction is design dependent. In space, this rare SEFI's likelihood can be made academically small by following a simple rule: only scrubbing when a configuration upset is detected. As a reasonable example, consider a readback rate of once per second, then with a configuration upset rate of about 4 per day (the GEO rate, see the next section), the reduction factor is more than four orders of magnitude (4/86400). Thus, for Virtex-4 FPGAs, we recommend using continuous readback instead of continuous scrubbing (or "blind" scrubbing).

In comparing these SEFI results with previous XRTC results on the Virtex II family [7], the FAR SEFI was certainly present, but was included in the SMAP SEFI basket; the GSIG and SCRUB SEFIs, if they exist in Virtex II, would have been counted in the POR SEFI basket.

## V. Rates in Selected Space Environments

CREME-96 was used to calculate device upset rates in selected space radiation environments for the configuration bits and as well as the total device SEFI rate. Table III gives the predicted rate of configuration upsets; note this is the average number of readback errors discovered in a day in these orbits. Not all configuration upsets result in design malfunction; usually it requires an average of ten or more – although the upsets-to-error is design dependent.

TABLE III
PREDICTED RATE OF CONFIGURATION UPSETS IN SELECTED ORBITS
Parameters: Solar Minimum Quiet, AP8max, z=1 μm and 100 mils of Al
Units are #/device-day

| Orbit | Altitude (km) | Incl* | XQR4V | | | | |
|---|---|---|---|---|---|---|---|
| | | | SX55 | FX60 | FX140 | LX200 | HI% |
| **LEO** | 400 | 51.6º | 0.73 | 0.69 | 1.61 | 2.03 | 69 |
| | 800 | 22.0º | 7.56 | 7.12 | 16.7 | 21.1 | 2 |
| **POLAR** | 833 | 98.7º | 6.02 | 5.67 | 13.3 | 16.8 | 22 |
| **MEO** | 1200 | 65.0º | 23.3 | 21.9 | 51.6 | 65.1 | 5 |
| **GEO** | 36,000 | 0º | 4.28 | 4.03 | 9.5 | 11.9 | 94 |

* Incl = Inclination HI% = fraction from heavy ions

Similarly, BRAM upset rates are given in Table IV. Upsets do not automatically imply system errors as upset mitigation like triplication or using Hamming codes can be employed in the design.

The upset rates for the user flip-flops are as important because these values are more likely to be corrupted by configuration upsets than by direct hits. For example, user flip-flops storing half zeros and half ones in GEO have a predicted direct-hit upset rate of $7.87 \times 10^{-7}$ per bit-day which works out to about one per week for all the flops in the largest device, the LX200, compared to ~100 configuration upsets per week. Either way, triple modular redundancy (TMR) with feedback path voting is quite effective at suppressing system errors when flip-flop and configuration upsets occur at space rates and are not allowed to accumulate. (Scrubbing fixes configuration upsets and the feedback voters synchronize the triplicated flip-flops.)

TABLE IV
PREDICTED RATE OF BRAM UPSETS IN SELECTED ORBITS
Parameters: Solar Minimum Quiet, AP8max, z=1 μm and 100 mils of Al
Units are #/device-day, assuming all bits are used

| Orbit | Altitude (km) | Incl* | XQR4V | | | | |
|---|---|---|---|---|---|---|---|
| | | | SX55 | FX60 | FX140 | LX200 | HI% |
| **LEO** | 400 | 51.6º | 0.72 | 0.52 | 1.24 | 0.75 | 84 |
| | 800 | 22.0º | 4.05 | 2.94 | 6.99 | 4.25 | 5 |
| **POLAR** | 833 | 98.7º | 4.00 | 2.90 | 6.90 | 4.20 | 37 |
| **MEO** | 1200 | 65.0º | 13.3 | 9.63 | 22.9 | 13.9 | 10 |
| **GEO** | 36,000 | 0º | 4.49 | 3.26 | 7.75 | 4.71 | 98 |

* Incl = Inclination HI% = fraction from heavy ions

SEFIs are expected somewhat infrequently - Table V lists the mean time between SEFIs in device-years. Note that only the POR and GSIG SEFIs cause an immediate outage while SMAP+FAR SEFIs cause readback and/or scrub problems which may be handled immediately or, in most cases, prudently deferred to a more convenient time. SEFI recovery involves reconfiguring the FPGA which does not require a power cycle, although that will certainly invoke the needed reconfiguration.

TABLE V
PREDICTED MEAN TIME TO SEFI IN SELECTED ORBITS
Parameters: Solar Minimum Quiet, AP8max, z=1 μm and 100 mils of Al
Years between events (on average).

| Orbit | Altitude (km) | Incl* | SEFIs | | | | |
|---|---|---|---|---|---|---|---|
| | | | POR | GSIG | SMAP+ | **TOTAL** | HI% |
| **LEO** | 400 | 51.6º | 1225 | 2161 | 1500 | **515** | 58 |
| | 800 | 22.0º | 100 | 114 | 112 | **36** | 13 |
| **POLAR** | 833 | 98.7º | 131 | 165 | 146 | **49** | 14 |
| **MEO** | 1200 | 65.0º | 32 | 37 | 35 | **11** | 3 |
| **GEO** | 36,000 | 0º | 225 | 560 | 290 | **103** | 91 |

* Incl = Inclination HI% = fraction from heavy ions
SMAP+ = SMAP & FAR SEFIs combined

## VI. Discussion

Virtex-4QV devices (V-grade, radiation-hardened) come with a guaranteed radiation specification for TID. In the case of the Virtex-4 family that level is 300 krad(Si) and is assured with individual wafer lot verification. Fabricating on thin-epitaxial wafers is intended to eliminate latchup susceptibility and the data presented here do show 'latchup immunity' using high bias and high temperature with the highest available LETs. With a high TID specification and no latchup problems, only the upset phenomena (SEFIs and SEUs) remain as potentially significant radiation problems.

The SEFI cross sections are low enough to be almost academic (not to mention difficult to measure). For those missions where they're not low enough, it is possible to

implement a dual-chip redundant system where each chip monitors the other for SEFI. In that case, it is possible to drive the system availability, in spite of SEFIs, to greater than eight nines, even considering large solar particle events.

The space upset rates given in the tables above may be sufficiently low for some missions and applications, particularly those that flush through a stream of data - where a bad pixel now and then is not a big concern. For other applications (like pyrotechnic- or rocket-control), upset mitigation techniques will be needed. In particular, full triple modular redundancy (TMR) of even a fairly large design is quite viable due to the large amount of logic resources and pins available in these devices and due to availability of the TMRTool software for correctly triplicating a design.

Comparing the upset susceptibilities across Virtex generations (see Ref.. 7 for Virtex II data), it is clear that the reduced area of the cell and increased charge sharing due to the closer spacing of charge collection nodes is winning over the reduction in critical charge to upset that accompanies lower core voltage. However, while per-bit rates in a given environment are going down, the growth in the number of bits more than compensates so that the device upset rates do increase with the reduction in feature sizes across the generations of FPGAs.

## VII. Conclusion

The Virtex-4QV family of SRAM-based reconfigurable FPGAs performed well in these heavy-ion and proton irradiations, exhibiting no SEL even at elevated temperature and spec-max voltages. Additional details are in Ref. 8, the XRTC report which is updated as more data is collected. All three device types exhibited low total SEFI susceptibility to heavy ions and protons with a resulting total rate of about one per 100 years in the geosynchronous radiation environment. This dataset shows that upsets of the configuration SRAM elements (as well as the user Block RAMs and the user flip-flops) are a significant concern. While the upset rates (a few bits per day in GEO) may be acceptable for some applications, critical applications will require design level mitigation, typically TMR plus configuration management. TMR assures correct operation in the presence of an upset and configuration management includes scrubbing to avoid the accumulation of upsets and SEFI detection to allow high system availability even if a rare SEFI should occur. Thus, with the combination of a TMR design and configuration scrubbing, the system error rate due to upsets can be reduced to below that of the SEFI rate for even the worst-case space environments.

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